88EM8011

Power Factor Correction Controller

Datasheet

Patents, Patents Pending Including US Pat. Nos. 7,266,001 and 7,292,013

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Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

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PRODUCT OVERVIEW

The Marvell® 88EM8011 is a high performance, low-cost with minimum component count Power Factor Correction (PFC) Controller. The device is used for Universal PFC front-end boost converter in systems or standalone products with power ranges between 10W–250W.

The 88EM8011 includes Marvell's patented (patent numbers 7266001B1 and 7292013B1) Mixed Mode Control (MMC) that ensures the lowest Total Harmonic Distortion (THD) in the industry. The average Continuous Conduction Mode (CCM) also is available as an option. The device has multiple switching frequency options to provide a variety of applications. The powerful adaptive driver self-adjusting feature allows flexibility for application in a wide range of MOSFET sizes.

The 88EM8011 controller improves the steady state and transient performance through Marvell's innovative Digital Signal Processing (DSP) solution. The combination of the MMC built on top of the DSP solution elevates industry standards for PFC controllers.

The proprietary adaptive over current protection ability ensures constant power constraint. The safety provisions include open loop and high voltage protection protocol.

The 8-pin SOIC and DIP packages provide simple application by minimizing requirements for external components as well as board space. This guarantees simple system design at a minimum cost making the 88EM8011 the best choice for any PFC application.

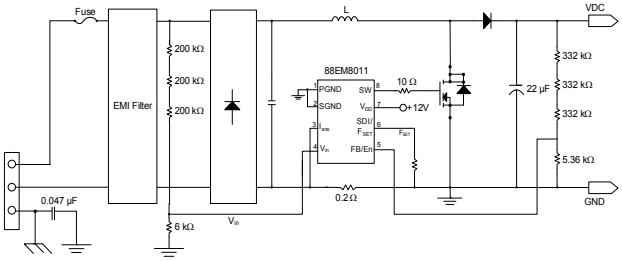
General Features

- Patented DSP control strategy
- Advanced MMC that utilizes CCM and Discontinuous Conduction Mode (DCM) operation
- High power factor and low harmonics performance for wide range of load conditions
- Fast dynamic performance during input and load transient state
- Adaptive over current protection for universal voltage level to provide constant power characteristic
- Open loop protection
- Adaptive gate driver for applications between 10W–250W
- Programmable switching frequency selective from 33.5 kHz up to 280 kHz
- Optimized total solution to reduce EMI and filter size
- Minimal external components required
- Thermal shutdown
- Built-in Under Voltage Lockout (UVLO)
- Over Voltage Protection (OVP)
- OInput line frequency range from 45Hz-65Hz

Applications

- Universal front-end PFC boost controller
- Electronic Ballast with PFC
- Any two-stage power supply with front-end PFC boost

PFC Controller Circuit Diagram



Marvell PFC Controller

Table 1: Feature Differences

Soft Start Control	Natural ramp	Level 1	Level 2	Level 3
Relative Ramp up Speed	No slow down	Slow down	Slow down	Slow down

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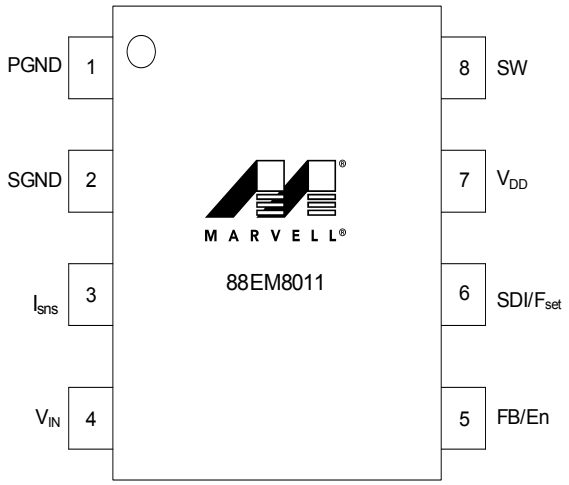
1 Signal Description

1.1 Pin Configuration

Figure 1: 8-Pin DIP Package—Top View



Pin #	Pin Name	I/O	Pin Function
1	PGND	GND	Power Ground
2	SGND	GND	Signal Ground
3	I_{sns}	I	Current Sense
4	V_{IN}	I	Voltage Input
5	FB/En	I	Feedback/Enable/Shutdown
6	SDI/F_{SET}	I/O	Serial Data Interface/Frequency Setting
7	V_{DD}	S	IC Supply Voltage
8	SW	O	Switch

1.2 Pin Description

This section provides pin descriptions for the 88EM8011.

Table 2: Pin Description

Pin #	Description
1	Power Ground Must be connected to the negative terminal of the output capacitor and to the source terminal of the boost MOSFET. To avoid any switching noise interruption on signal processing, PGND and SGND remain isolated inside the IC.
2	Signal Ground Must be connected to the power ground on the power board. Quiet ground is available at the negative terminal of the output bulk capacitor. SGND has dedicated trace and connections and provides noiseless environment for the signal processing.
3	Current Sense Sense resistor varies from 0.05Ω at 250W rated power to 0.2Ω at 62.5W rated power. Used for current shaping and for over current protection.
4	Voltage Input Connects to resistive divider at input AC line “phase” to GND. Voltage applied is a half rectified sine wave scaled down by the input resistive divider. Voltage compared with a threshold reference is used to detect the zero-cross location of the input sine wave and synthesize (regenerate) the input sine wave. This sine wave is used to generate the current reference.
5	FB/En connects to the output resistive divider. FB/En serves as the Feedback as well as Enable the chip. It has an open collector connection. **Feedback**: FB It is scaled down of the output voltage 450V/2.5V. Output voltage regulation at 100% rated V_{FB_REG} = 2.5V (ADC process). Enable threshold detection at V_{FB_En} (Table 5). Transition from soft start to normal regulation at 87.5% rated V_{FB}. Over voltage shuts down at 107% rated V_{FB}. **Enable/Shutdown**: En At V_{FB}>V_{FB_En} (Table 5) IC is enabled. Pulling this pin to low or V_o<V_{FB_ShDn} (Table 5) disables the chip back to the sleep mode.
6	SDI/F_{SET} is a multi-purpose I/O, used to set frequency, and read/write (R/W) binary registers on DSP core. **Frequency Setting**: F_{SET} Connects a predefined external resistor from the pin to GND. **Serial Data Interface**: SDI Used to R/W on the registers through a single-wire SDI.
7	IC Supply Voltage Nominal voltage is typical 12V and the Under Voltage Lock Out (UVLO) for V_{DD} <V_{DD_UVLO} (Table 5). Start voltage of IC is V_{DD_On} (Table 5) and maximum voltage is 16V (Table 5) (clamped by type of internal zener protection at this pin).
8	Switch PWM gating signal for the boost switch. Connects to the gate of external boost MOSFET. It is the DSP core output for ON/OFF time buffered through the internal adaptive driver.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings[1]

NOTE: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Units
V_{DD}	Power Supply (Voltage to PGND=SGND)	-0.3	18	V
VI_{sns}	Voltage at I_{SNS} pin	-0.5	3	V
$V_{FSET/SDI}$	Voltage at $F_{SET/SDI}$ pin	-0.3	5.5	V
V_{IN}	Voltage at V_{IN} pin	-0.3	5.5	V
$V_{FB/En}$	Voltage at $V_{FB/EN}$ pin	-0.3	5.5	V
I_{SW}	Driver Current (Instantaneous Peak)		2	A
θ_{JA}	Thermal Resistance SOIC-8		156.5	°C/W
	Thermal Resistance DIP-8		89.5	°C/W
T_A	Operating Ambient Temperature Boundary[2]	-40	85	°C
T_J	Junction Temperature		125	°C
T_{STOR}	Storage Temperature Range	-65	150	°C
V_{ESD}	ESD Rating[3]		2	kV

1. Exceeding the absolute maximum rating may damage the device.
2. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
3. Devices are ESD sensitive. Handling precautions recommended. Human Body model, 1.5 kΩ in series with 100 pF.

2.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ	Max	Units
T_A	Operating Ambient Temperature[2]	-40		85	°C
T_J	Junction Temperature	-20		125	°C

1. This device is not guaranteed to function outside the specified operating temperature range.
2. Over the –40°C to 80°C operating temperature ranges are assured by design, characterization, and correlation with statistical process controls.

2.3 Electrical Characteristics

Table 5: Electrical Characteristics

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Supply						
V_{DD}	Supply Voltage		8.0	12	16	V
V_{DD_On}	V_{DD} Power On Threshold			12.92		V
V_{DD_UVLO}	V_{DD} Power Off Threshold (UVLO)	After V_{DD} is powered up and running		8.0		V
$V_{DD\_UVLO\_Hys}$	V_{DD_UVLO} Hysteresis		4.8		5	V
I_{DD_SLP}	V_{DD} Sleep Current	V_{DD} = 12V V_{En} < 0.2V		166.5		µA
I_{DD_OP}	V_{DD} Operating Current	V_{DD} = 12V; V_{En} > 0.25V C_{Gate} = 1nF F_{SW} = 140kHz V_{IN}=0		5.94		mA
Thermal Shutdown						
T_{SD}	Thermal Shutdown		150			°C
T_{SD_Hys}	Hysteresis for Thermal Shutdown		25			°C
Adaptive Output Gate Driver						
V_{G_Hi}	Minimum Gate High Voltage[1]	V_{DD} = 12V	>8.5			V
V_{G_Lo}	Maximum Gate Low Voltage[2]				<3.0	V
RDS_On	Gate Drive Resistance (For each array PMOS)	Sourcing 75mA T=25°C		20.2		Ω
	Gate Drive Resistance (For each array NMOS)	Sinking 20mA T=25°C		16.6		Ω
Isw_Pk	Driver Peak Current	C_{Gate} = 10 nF V_{DD} = 12 V	2.0			A
t_r	Rise Time	C_{Gate} = 1 nF		100		ns
		C_{Gate} = 10 nF		150		ns
t_f	Fall Time	C_{Gate} = 1 nF		100		ns
		C_{Gate} = 10 nF		150		ns
D_{Max}	Maximum Duty Cycle				97	%

Table 5: Electrical Characteristics (Continued)

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D_{Min}	Minimum Duty Cycle		3.0			%
Feedback/Enable/Overvoltage						
V_{FB_REG}	Normal Regulation Reference	At boost output rated voltage		2.5		V
V_{FB_En}	V_{FB} at Enable Threshold	IC powered on by V_{DD_On}. Transition from sleep mode to IC enable at Enable Threshold of V_{FB_En}		0.278		V
V_{FB_ShDn}	V_{FB} at Shutdown Threshold	IC powered on by V_{DD_On}. Transfer from IC enable to sleep mode at Shutdown Threshold of V_{FB}		0.223		V
$V_{FB\_En\_Hys}$	V_{FB} at Enable Hysteresis	--		--		V
V_{FB_OVP}	Over Voltage Protection Threshold	At 107% of boost output rated voltage.		2.71		V
$V_{FB\_OVP\_Hys}$	OVP Hysteresis				0.108	V
Current Sensing and Current Protection[3]						
V_{Iover_Th1}	Over Current Threshold Zone 1[4]	Peak value of half-sine voltage at V_{IN}: $1.26<V_{IN}<1.89V_{pk}$[5]		397		mV
V_{Iover_Th2}	Over Current Threshold Zone 2[4]	Peak value of half-sine voltage at V_{IN}: $1.89<V_{IN}<2.59V_{pk}$[6]		329		mV
V_{Iover_Th3}	Over Current Threshold Zone 3[4]	Peak value of half-sine voltage at V_{IN}: $2.59< V_{IN}<3.43V_{pk}$[7]		269		mV
V_{Iover_Th4}	Over Current Threshold Zone 4[4]	Peak value of half-sine voltage at V_{IN}: $3.43<V_{IN}<3.85V_{pk}$[8]		202		mV
Switching Frequency Oscillator[9]						
	Initial Accuracy				15	%
F_{SW1}	Frequency/ Set Up 1 (Average Mode)	R_{FSET} = 10kΩ		33.5		kHz
	(Mixed Mode)		33.5		67	kHz

Table 5: Electrical Characteristics (Continued)

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SW2}	Frequency/ Set Up 2 (Average Mode)	R_{FSET} = 35kΩ		70.8		kHz
	(Mixed Mode)		71		142	kHz
F_{SW3}	Frequency/ Set Up 3 (Average Mode)	R_{FSET} = 95kΩ		140		kHz
	(Mixed Mode)		140		280	kHz
Serial Data Interface (SDI)[10]						
	SDI Maximum Voltage Level		2.5	3.3	5	V
	SDI Maximum Clock Frequency			1	TBD	MHz

1. Considering the voltage drop on the internal driver MOSFET during current sourcing.
2. Considering the voltage drop on the internal driver MOSFET during current sinking.
3. To achieve almost constant power limit for the universal input range, current protection self-adjusts thresholds in four zones of input voltage levels. A margin of 50% compared to the rated current is considered for the threshold current values.
4. Threshold of negative voltage drop across R_{sns} due to instantaneous current
5. With input divider ratio of 6/606, these values are equivalent to 90 V_{rms}<V_{line}<135 V_{rms}.
6. With input divider ratio of 6/606, these values are equivalent to 135 V_{rms}<V_{line}<185 V_{rms}.
7. With input divider ratio of 6/606, these values are equivalent to 185 V_{rms}<V_{line}<245 V_{rms}.
8. With input divider ratio of 6/606, these values are equivalent to 245 V_{rms}<V_{line}<275 V_{rms}.
9. Switching frequency is adjustable in three set ups by insertion of the predefined resistors at F_{SET} to GND.
10. SDI option from SDI/F_{SET} pin is used for writing on the selective registers by binary codes to select the optional functions. This option is not accessible for the end user.

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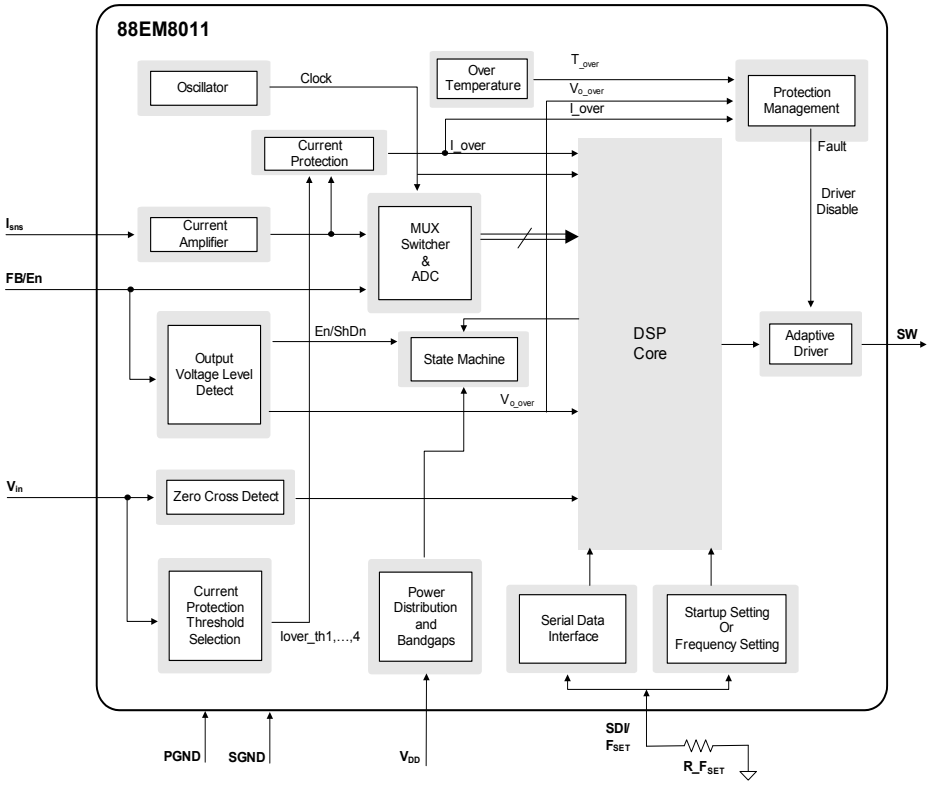
3 Functional Description

3.1 Overview

The 88EM8011 is a high performance, low-cost with minimum component count Power Factor Correction (PFC) Controller. The device is used for Universal PFC front-end boost converter in systems or standalone products with power ranges between 10W–250W. The high performance of 88EM8011 is accompanied with its small size and simplicity of application. Figure 2 shows the top level block diagram.

Figure 2: Top Level Block Diagram



Note

- R_F_{SET} is the frequency setting resistor.
- I_{over}_th1,...4 are the over current threshold at different regions of the universal input voltage.
- I_over, V_{o_over}, and $T_{\_over}$ are the over current, over voltage, and over temperature signals respectively.

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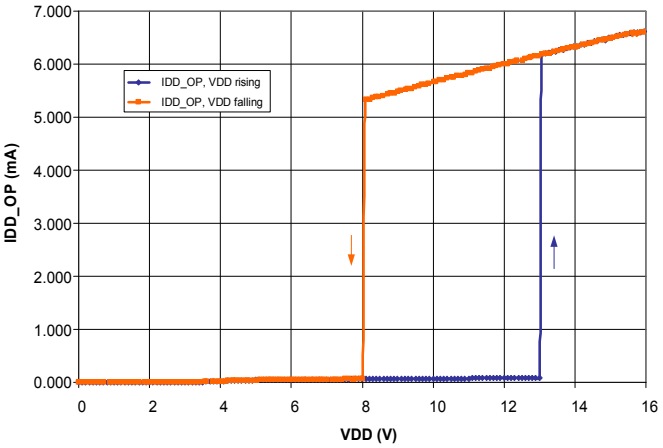
4 Functional Characteristics

The following applies unless otherwise noted: V_{IN} = 60 Hz half-wave sinusoidal from 0V to the peak voltage (V_{pk}) given in the test conditions of each graph.

All measurement readings are typical.

4.1 V_{DD} Waveforms

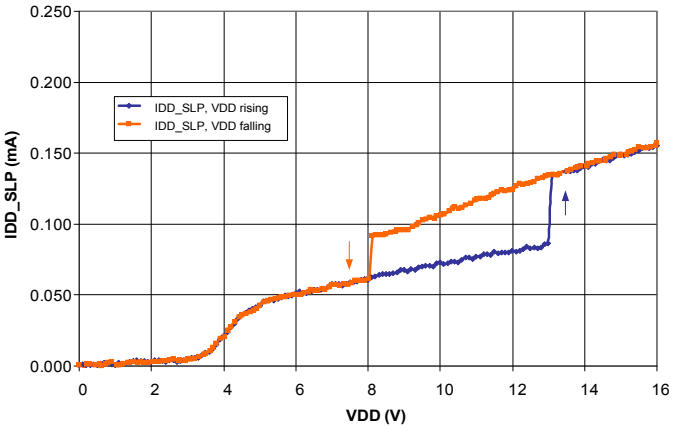
Figure 12: I_{DD} Operation (I_{DD}_OP) vs. V_{DD}



Test Conditions:

- V_{IN} = $3V_{pk}$
- F_{SW} = 140 Hz
- V_{FB} = 2.4V
- C_{Gate} = 1 nF
- V_I_{sns} = 0V

Figure 13: I_{DD} Sleep (I_{DD}_SLP) vs. V_{DD}

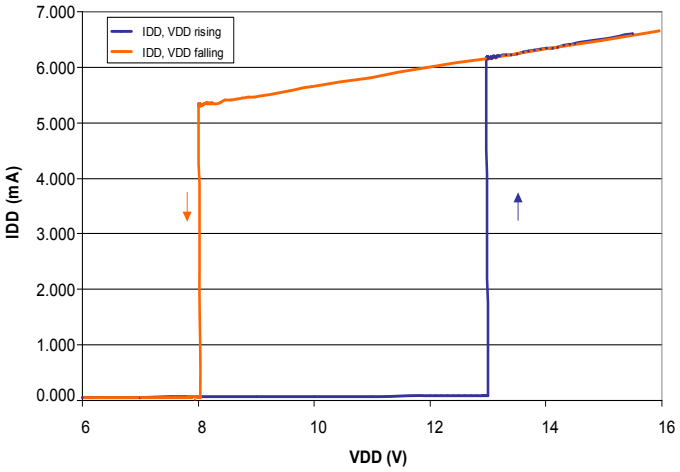


Test Conditions:

- V_{IN} = 0V
- F_{SW} = 140kHz
- V_{FB} = 0V
- C_{Gate} = 1 nF
- V_I_{sns} = 0V

NOTE: V_I_{SNS} is the voltage on the ISNS pin.

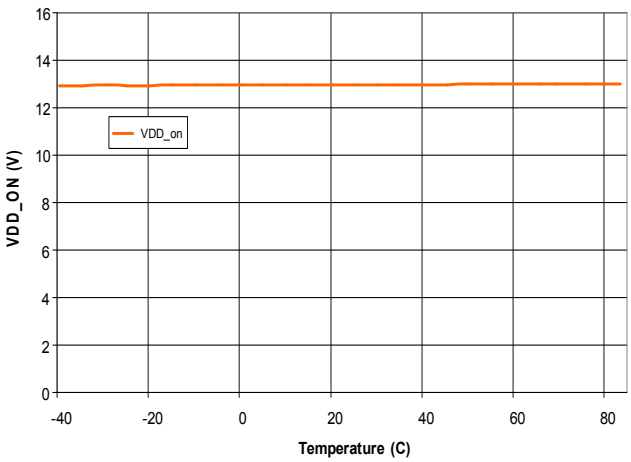
Figure 14: I_{DD} vs. V_{DD} (V_{DD_ON} Threshold)



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 140kHz
- V_{FB} = 2.4V
- V_Isns = 0V
- C_{Gate} = 1nF

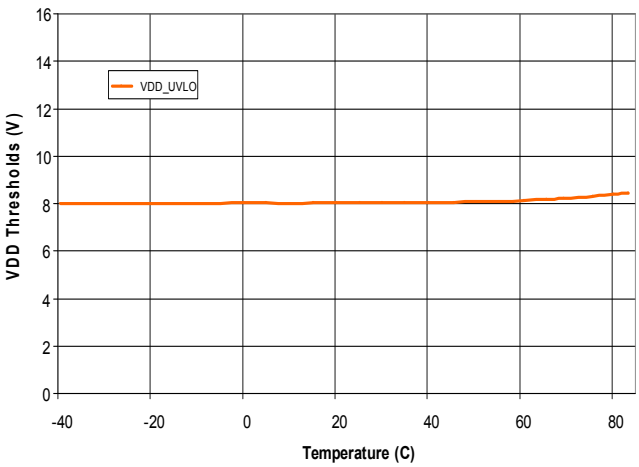
Figure 15: Power On Threshold (V_{DD}_on) vs. Temperature



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 140kHz
- V_{FB} = 2.4V
- C_{Gate} = 1 nF
- V_Isns = 0V

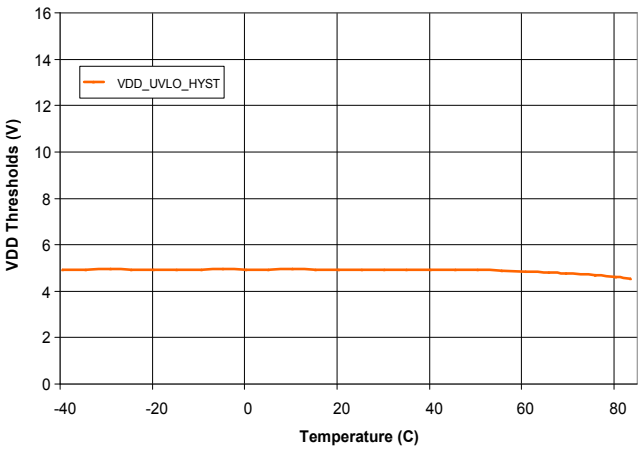
Figure 16: Power Off Threshold of V_{DD} (V_{DD}_UVLO) vs. Temperature



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 140kHz
- V_{FB} = 2.4V
- C_{Gate} = 1 nF
- V_Isns = 0V

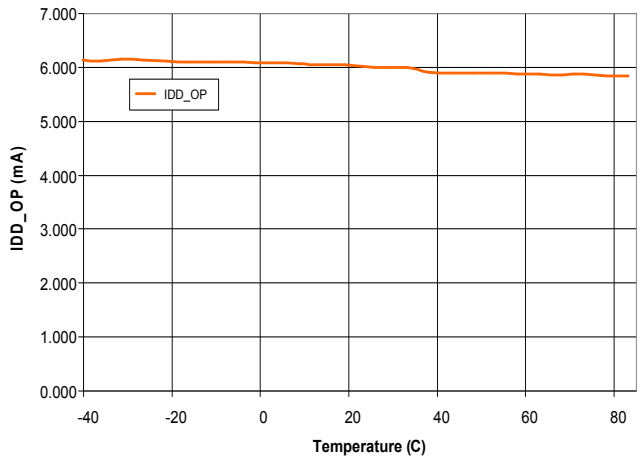
Figure 17: V_{DD} UVLO Hysteresis (V_{DD}_UVLO_Hys) vs. Temperature$_I$



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 140kHz
- V_{FB} = 2.4V
- C_{Gate} = 1 nF
- V_Isns = 0V

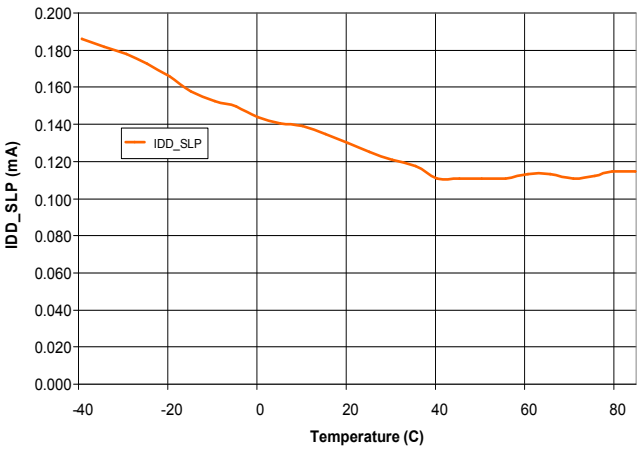
Figure 18: I_{DD} Operation (I_{DD}_OP) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_I_{sns} = 0V
- V_{IN} = $2V_{pk}$
- F_{SW} = 140kHz
- V_{FB} = 2.4V
- C_{Gate} = 1 nF

Figure 19: I_{DD} Sleep Current (I_{DD}_SLP) vs. Temperature

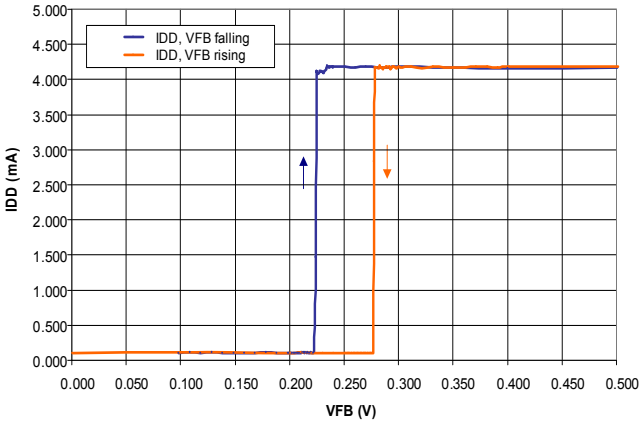


Test Conditions:

- V_{DD} = 12V
- V_I_{sns} = 0V
- V_{IN} = 0V
- F_{SW} = 140kHz
- V_{FB} = 0V
- C_{Gate} = 1 nF

4.2 V_{FB} Waveforms for Enable/Shutdown

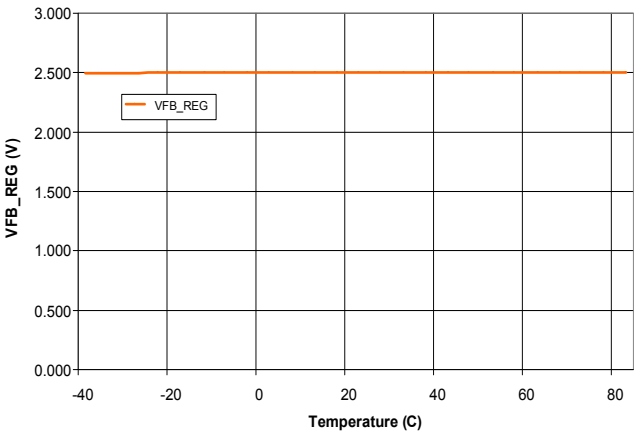
Figure 20: I_{DD} vs. V_{FB} (Enable Threshold)



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 37.5 kHz
- V_{IN} = 0V
- C_{Gate} = 1 nF
- V_I_{sns} = 0V

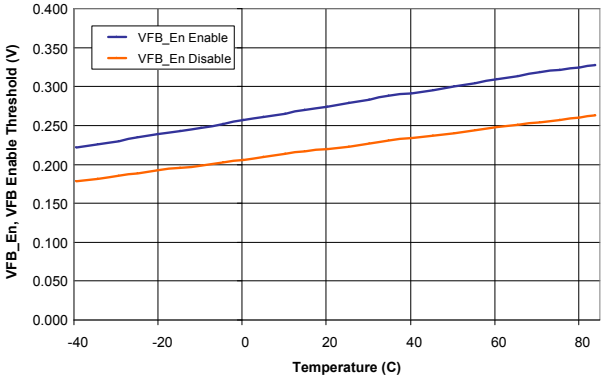
Figure 21: Normal Regulation Reference (V_{FB}_REG)vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_I_{sns} = 0V
- V_{IN} = $2V_{pk}$
- F_{SW} = 37.5 kHz
- V_{FB} = 0V
- C_{Gate} = 1 nF

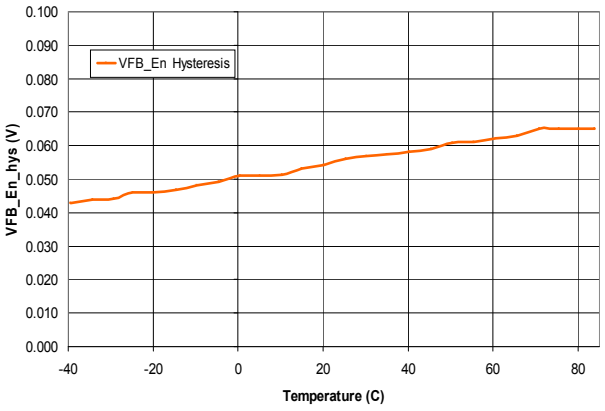
Figure 22: V_{FB} Enable Threshold (V_{FB}_En) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 37.5 kHz
- V_{IN} = 0V
- C_{Gate} = 1 nF
- V_I_{sns} = 0V

Figure 23: V_{FB} Enable Hysteresis (V_{FB}_En_Hys) vs. Temperature

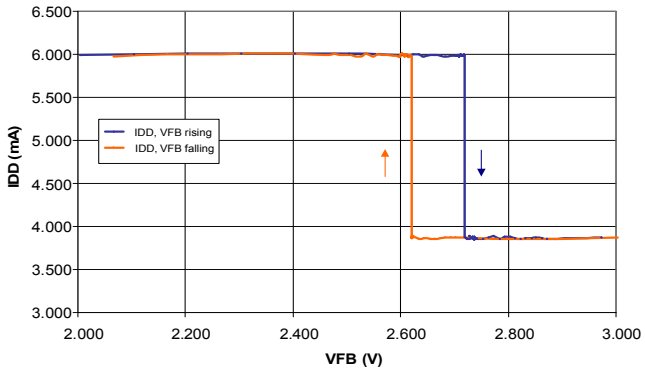


Test Conditions:

- V_{DD} = 12V
- F_{SW} = 37.5 kHz
- V_{IN} = 0V
- C_{Gate} = 1 nF
- V_I_{sns} = 0V

4.3 V_{FB} Waveforms for Over Voltage Protection

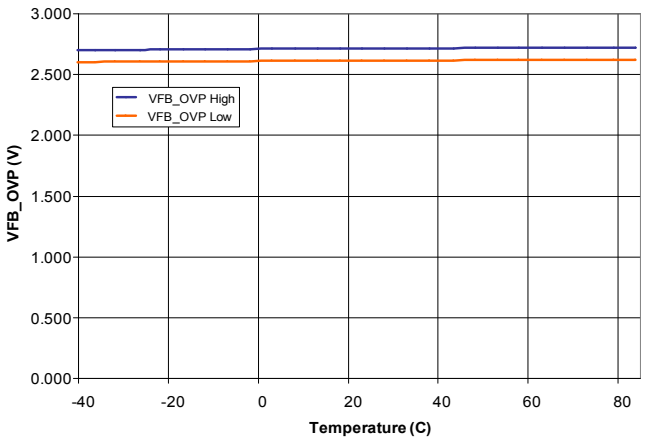
Figure 24: I_{DD} vs. V_{FB} (OVP Threshold)



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 140kHz
- V_{IN} = 0V
- C_{Gate} = 1 nF
- V_I_{sns} = 0V

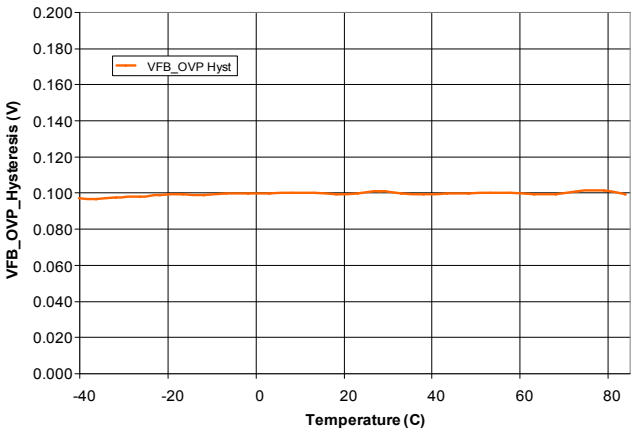
Figure 25: Over Voltage Protection Threshold (V_{FB}_OVP) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 140kHz
- V_{IN} = 0V
- C_{Gate} = 1 nF
- V_I_{sns} = 0V

Figure 26: Over Voltage Protection Hysteresis (V_{FB}_OVP_Hys.) vs. Temperature

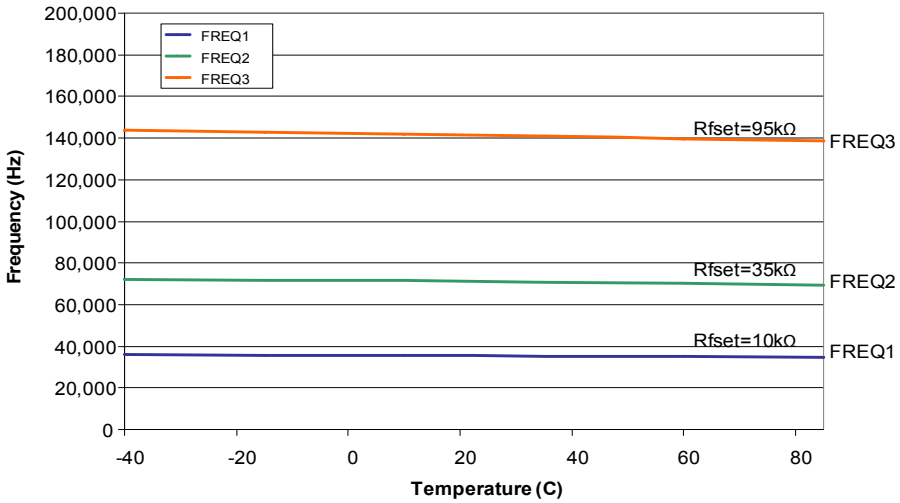


Test Conditions:

- V_{DD} = 12V
- F_{SW} = 140kHz
- V_{IN} = 0V
- C_{Gate} = 1 nF
- V_I_{sns} = 0V

4.4 Switching Frequency Waveform

Figure 27: Switching Frequency vs. Temperature

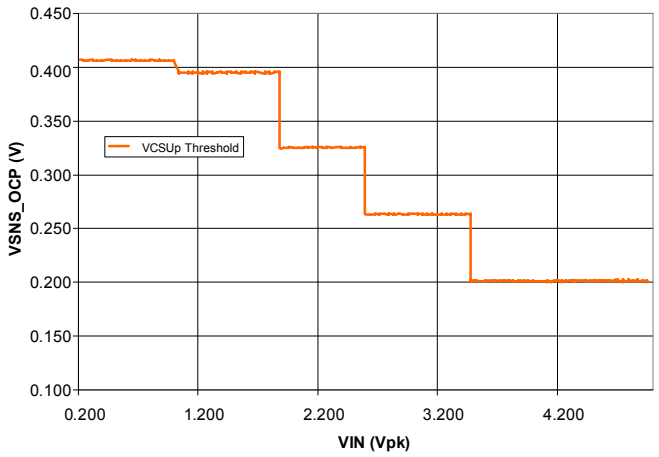


Test Conditions:

- V_{DD} = 12V
- V_I_{sns} = 0V
- V_{IN} = 0V
- V_{FB} = 2.4V
- C_{Gate} = 1 nF

4.5 Over Current Threshold Waveform

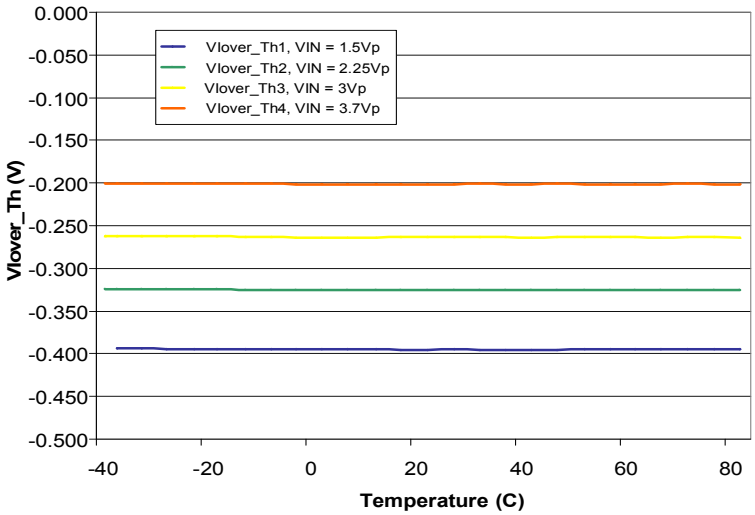
Figure 28: Over Current Threshold (I_{over}) vs. Input Voltage V_{IN} Peak Value)



Test Conditions:

- V_{DD} = 12V
- V_{FB} = 2.4V
- F_{SW} = 140kHz
- C_{Gate} = 1 nF

Figure 29: Over Current Threshold (VI_{over}_Th) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{FB} = 2.4V
- F_{SW} = 140kHz
- C_{Gate} = 1 nF

5 Typical Characteristics

5.1 Input Sinusoidal Voltage

Figure 30 shows the input sinusoidal voltage and current at steady state for full load (60W) and 110Vrms input voltage for circuit diagram.

Figure 30: Input Sinusoidal at 110Vrms

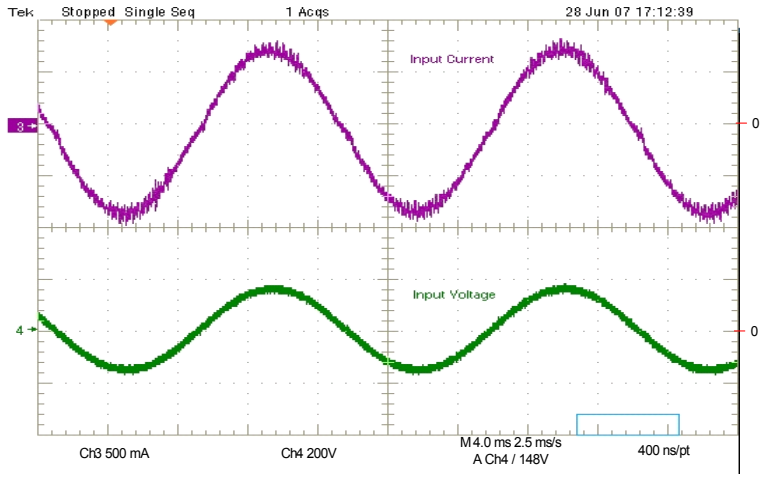
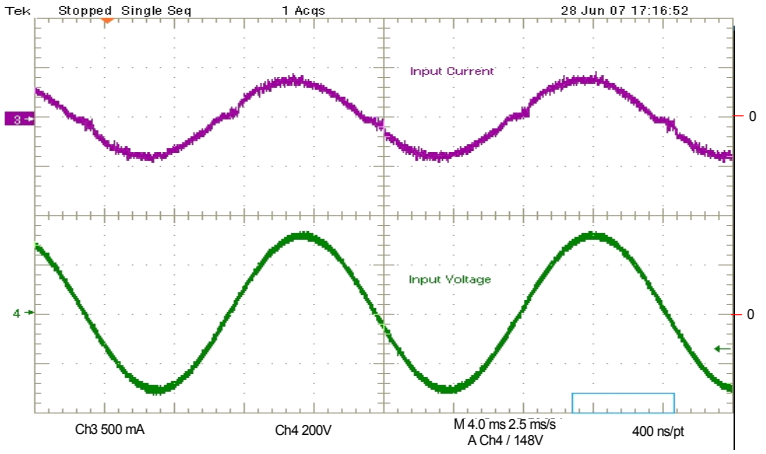


Figure 31 shows the input sinusoidal voltage and current at steady state for full load (60W) and 220Vrms input voltage for circuit diagram.

Figure 31: Input Sinusoidal at 220Vrms



5.2 Startup with Soft Start

Figure 32 shows the startup at 110Vrms input voltage and full load (60W) and with natural soft start slope.

Figure 32: Startup at 110Vrms

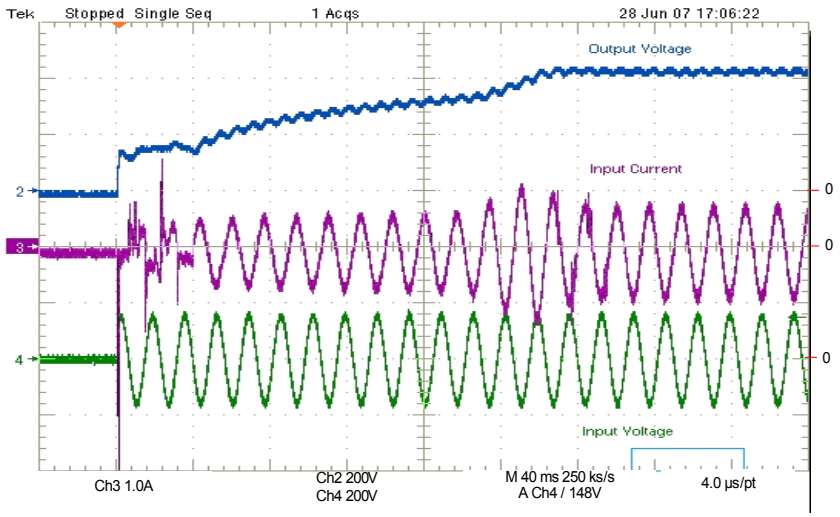
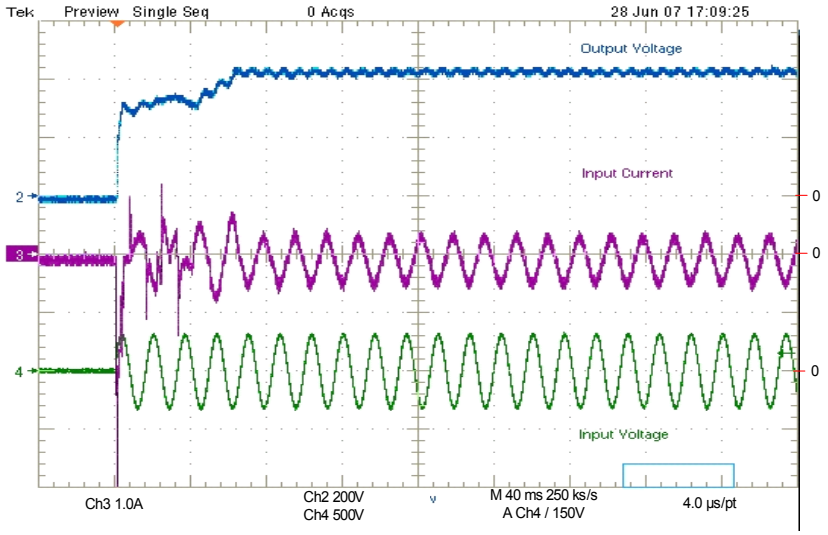


Figure 33 shows the startup at 220Vrms input voltage and full load (60W) and with natural soft start slope.

Figure 33: Startup at 220Vrms



5.3 Load Transient

Figure 34 shows the load transient test from full to half load and vise versa at 110Vrms input voltage for the circuit diagram. Overshoot and undershoot during transient remain below 10%.

Figure 34: Load Transient at 110Vrms

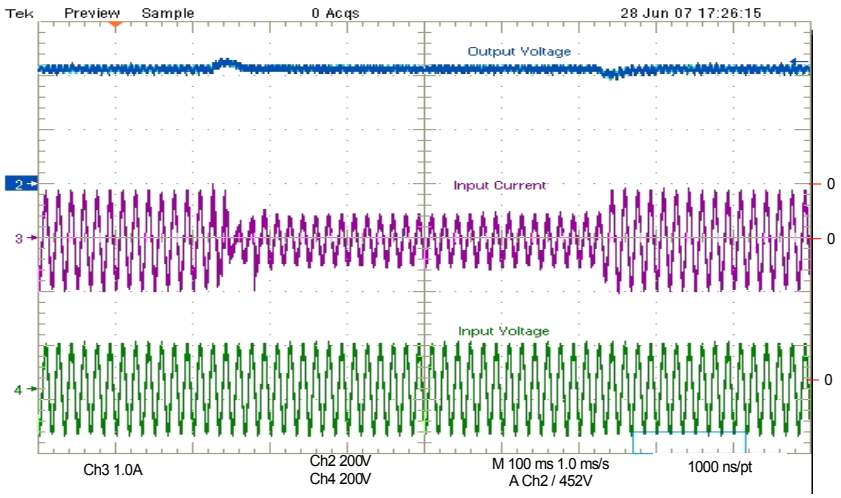
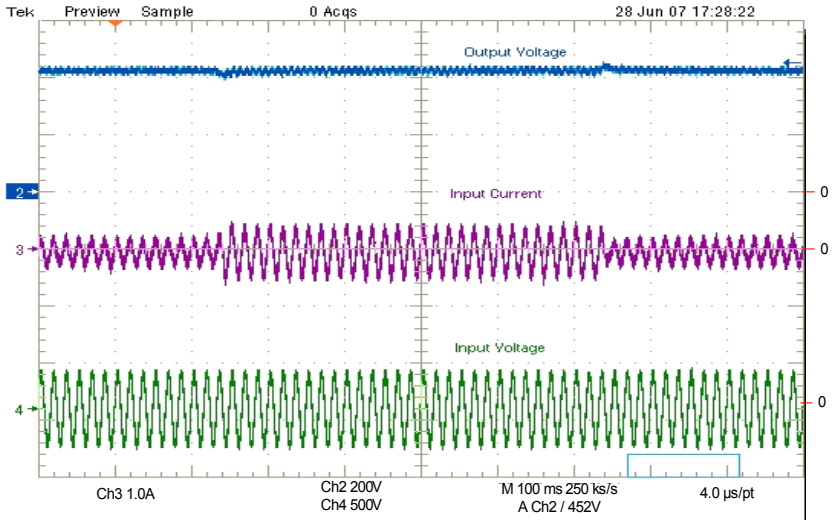


Figure 35 shows the load transient test from full to half load and vise versa at 220Vrms input voltage for the circuit diagram. Overshoot and undershoot during transient remain below 8%.

Figure 35: Load Transient at 220Vrms



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6 Applications Information

6.1 PFC Boost Performance with 88EM8011 PFC Controller IC

Marvell's mixed mode control technique improves performance of the boost converter by adopting advantages of both PWM and PFM control techniques. Operation mode changes from PWM near peak area of the line cycle with fixed frequency, to PFM near the zero crossing area. The frequency for PFM mode is increased from the base frequency of PWM mode up to two times the base frequency. The boost converter achieves:

- Reduced HF ripple current and filter size compared to the conventional DCM and Critical Mode
- Reduced switching loss and improved efficiency compared to the CCM
- Improved PF and reduced THD for the line current compared to the DCM or CCM
- Smaller value of boost inductor compared to the conventional CCM boost converters

Other advanced benefits for the boost power board include:

- Efficient safe charge pump for any applicable MOSFET on the board (10W to 250W) by the powerful smart adaptive driver.
- Selective frequency range of operation from 37.5 kHz up to as high as 300 kHz based on application.
- Adaptive over current protection that detects voltage level of the universal input and self adjusts the current limit reference for an almost constant source power.
- Precise output regulation with low output tolerance.
- Simplified application and minimized component count resulting in lower cost and size of the power board.
- No zero current detection. Secondary winding on the boost inductor can be used for the VDD supply in a standalone front-end PFC product.
- Boost output Over Voltage Protection (OVP).

Only a current sense resistor with input and output resistive voltage dividers provide all the required signals from the power board to the controller IC. The following sections give the guidelines for choosing these components.

6.2 Current Sense Resistor

The voltage drop on the current sense resistor should be kept very small. The sense resistor is calculated based on the input rated power and a minimum AC voltage of 90Vrms for a fixed voltage drop of 140 mV at the rated current. The voltage sensed on pin I_{sns} at different loadings is independent of the rated current. The IC current loop responds to the normalized value (percentage) of the current independent of the power board rated power. Table 6 shows the current sense resistor selection guide based on the rated power boost power board. The rated power dissipation of the sense resistor is selected based on boost-rated power with enough margin (1W resistor for 60W application).

Table 6: Current Sense Resistor Selection

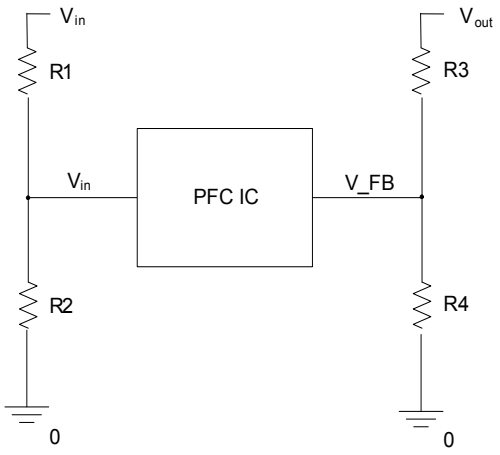
Input Rated Power (W)	62.5	125	187.5	250
Current Sense Resistor (Ω)	0.2	0.1	0.065	0.05

6.3 Input/Output Voltage Divider

To select input/output dividers, an appropriate combination based on the size and voltage/power rating of resistors should be considered.

For a 450V DC bus application, the output divider consists of R3 = 3x332 kΩ at high voltage side and R4 = 5.60 kΩ at the IC pin FB. Input divider consists of R1 = 3x200 kΩ and R2 = 6.04 kΩ at the IC pin V_{IN}.

Figure 36: Input/Output Voltage Divider



Calculations inside the IC are based on the predefined specific relation between input/output sensed voltages.

To save this ratio the following relation should always be satisfied:

$$\frac{R2 \cdot R3}{R1 \cdot R4} = constant$$

By changing the output divider ratios (reference constant 2.5V), the output voltage regulation should be adjusted from 450V to 200V (considering that output should always be greater than peak of input voltage). For instance, with fixed R3 = 996 kΩ, choosing R4 = 6.26 kΩ gives sensed voltage of 2.5V at V_{out} = 400V. R4 =12.60 kΩ gives the sensed voltage of 2.5V at V_{out} =200V.

With an input voltage of 110 Vrms, adjustment for the output divider ratio and DC bus regulated voltage are summarized in Table 7.

Table 7: Output Voltage Regulation (R2*R3)/(R1*R4) = constant

V_{out} (V)	R1 (kΩ)	R2[1] (kΩ)	R3 (kΩ)	R4[1] (kΩ)	Kin = R2/R1	Kout = R4/R3	Kin/Kout
450	600	6.04	996	5.60	0.0100	0.0056	1.8
400	600	6.80	996	6.26	0.0113	0.0063	1.8
350	600	7.69	996	7.15	0.0129	0.0072	1.8
300	600	9.00	996	8.35	0.0151	0.0084	1.8
250	600	10.90	996	10.00	0.0181	0.0101	1.8
200	600	13.70	996	12.60	0.0228	0.0127	1.8

1. These given values are based on the nearest standard resistor values.

NOTE: The resistor values in this table are only suggested values. They can change as long as the main mandatory ratio is satified.

6.4 Gate Circuit

A 20Ω resistor is connected between the SW pin to the gate of the external MOSFET switch for the purpose of dampening the current being charged or discharged from the input capacitor of the MOSFET.

6.5 Schematic and Layout Guidelines

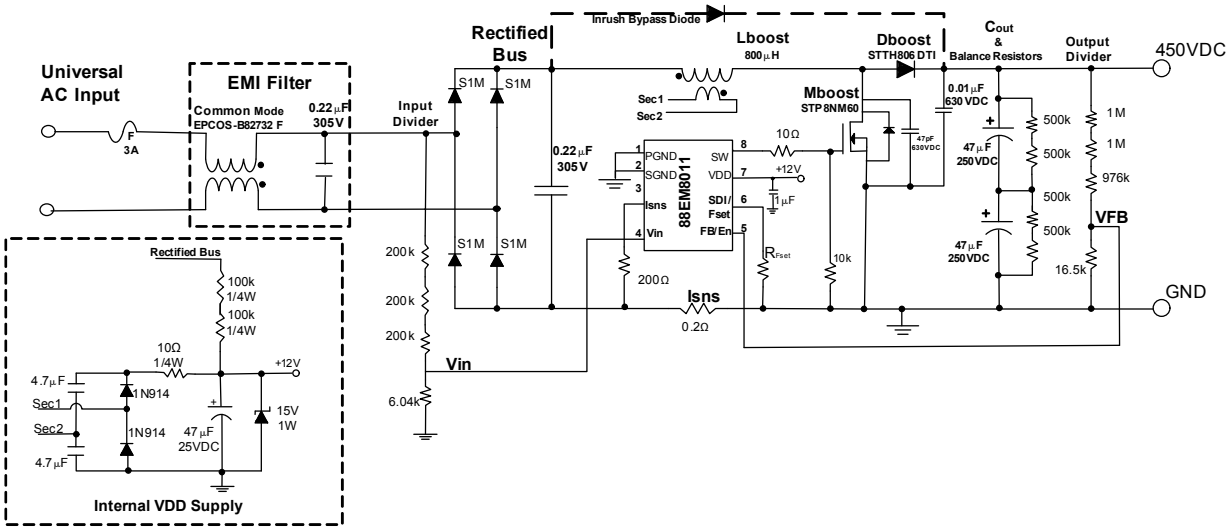
The following guidelines are the recommended points that help increase the boost power board performance.

1. The output loop consisting of the boost MOSFET, boost diode, and the output bulk capacitor is subject to fast rise of switching current. The length of this loop must be minimized on the power board layout design. Any parasitic inductance in this path in conjunction with the MOSFET parasitic capacitor could cause unwanted oscillations. These unwanted oscillations in addition to extra stress on the devices are a source of loss and reduced efficiency.
2. Output electrolytic capacitor is selected based on the output ripple limit or the hold-on time of the DC voltage bus. ESR of the output capacitor must be very low to avoid power loss and heat dissipation.
3. For a 450V DC bus, a minimum voltage rating of 500V for the output capacitor is required. If the cost consideration encourages using two electrolytic capacitors of 250V in series, then precautions must be kept in mind. DC leakage current due to the material and age of the capacitors is unavoidable. To avoid unbalance voltage across the series capacitors due to the leakage, a resistor network with connection of the center point to the midpoint of the capacitors is recommended.
4. The bulk electrolytic capacitor cannot bypass the very fast switching oscillation. To reduce stress and power loss due to the switching oscillations, a high voltage polypropylene capacitor of small value about 10 nF to 33 nF is recommended. This capacitor should directly be laid out from cathode of the boost diode to the source of boost MOSFET.
5. Some designers preferably add a high voltage ceramic capacitor of about 50–100 pF across the boost MOSFET to bypass the EMI frequency oscillations. However, the output capacitor of the MOSFET could partially perform the same duty. This external capacitor in many designs is ignored.
6. To reduce the reverse recovery stress of the boost diode on the MOSFET, switch turn on is recommended to use an ultra fast or recovery-less boost diode. Lower current rating with

smaller die size is preferred. However, during the power on, the inrush current through this diode to charge the bulk electrolytic capacitor could exceed the safety ratings of the diode. In such cases, a general purpose fast recovery diode across the boost inductor plus boost diode is added. This inrush bypass diode could help avoid the saturation of the inductor and any damage to the boost diode during the power on.

Figure 37 shows the PCB schematic with an internal V_{DD} supply circuitry from a secondary winding on boost inductor.

Figure 37: Circuit Diagram of 60W PFC Boost with 88EM8011 Controller



6.5.1 PC Board Layout Example

The following layout example is based on the schematic in Figure 38.

- Actual board size = 3650 mil x 1100 mil; Area = 4.015 in^2
- Total copper layers = 2 (Top Layer, Bottom Layer)

Figure 38: 88EM8011 PCB Schematic

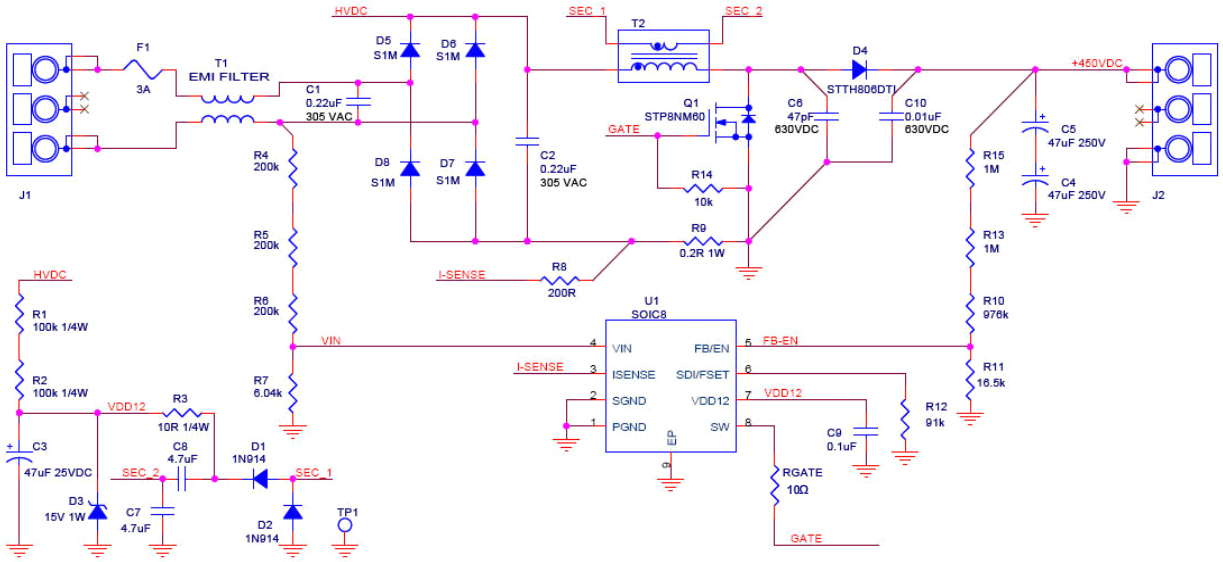


Figure 39: Top Layer Silk Screen (Not to scale)

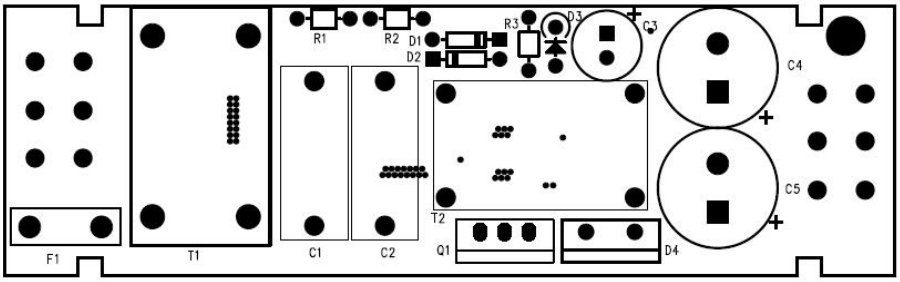


Figure 40: Top Layer Copper Traces (Not to scale)

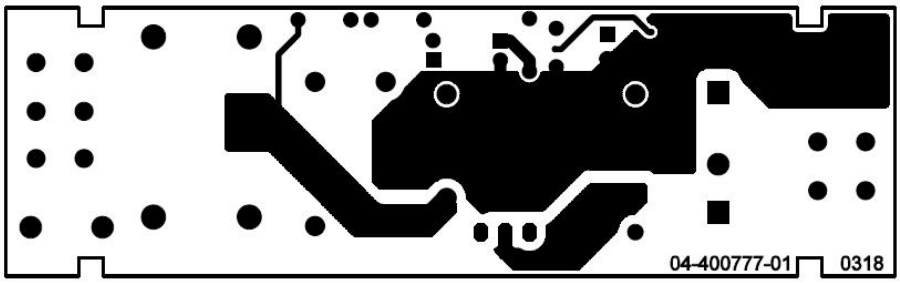


Figure 41: Bottom Layer Copper Traces (Not to scale)

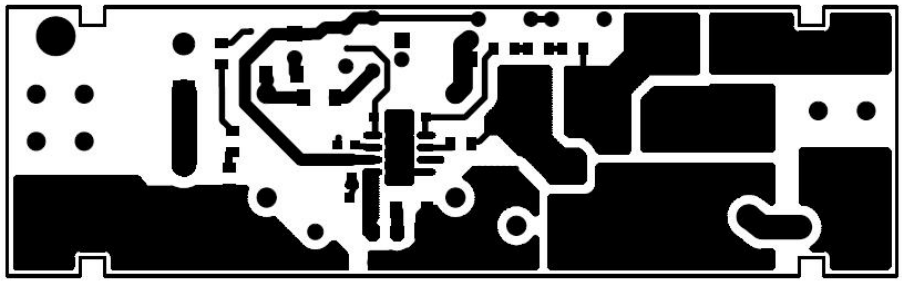
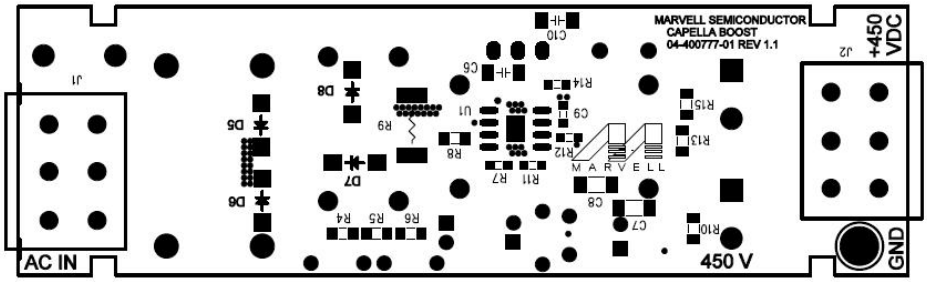


Figure 42: Bottom Layer Silk Screen (Not to scale)



6.6 Bill of Materials

Table 8: 88EM8011 BOM

Item	Qty	Ref	Manufacturer Part #	Manufacturer	Description
1	2	C1,C2	B32922C3224M	EPCOS Inc.	CAP .22UF 305VAC EMI SUPPRESSION
2	1	C3	EEU-FC1E470	Panasonic	CAP47UF 25V ELECT FC RADIAL
3	2	C4,C5	EEU-EB2E470	Panasonic	CAP 47UF 250V ELECT EB RADIAL
4	1	C6			NO LOAD
5	2	C7,C8	ECJ-3YB1E475K	Panasonic	CAP 4.7UF 25V CERAMIC X5R 1206
6	1	C9	ECJ-1VB1E104K	Panasonic	CAP CERAMIC 0. 1UF 25V X5R 0603
7	1	C10			NO LOAD
8	2	D1,D2	1N914TR	Fairchild	DIODE SS HI COND100V 200MA DO-35
9	1	D3	1N4744A-TP	Micro Commercial	DIODE ZENER 1W 15V D041
10	1	D4	STTH806DTI	ST Microelectronics	DIODE BOOST 600V 8A TO-220AB
11	4	D5,D6,D7,D8	S1M-13	Diodes Inc.	Glass Passivated Diode 1000V 1A SM
12	1	F1	F1001CT-ND	LittleFuse	FUSE 3A/350V FAST SMT EBF
13	2	J1,J2	ED4101/3-KD	OST	TERMINAL BLOCK 5MM 3POS PCB
14	1	Q1	STP8NM60	ST Microelectronics	MOSFET N-CHAN 650V 8A TO-220
15	2	R1,R2	ERD-S2TJ104V	Panasonic	RES 100K OHM CARBON FILM 1/4W 5%
16	1	R3	ERD-S2TJ100V	Panasonic	RES 10 OHM CARBON FILM 1/4W 5%
17	3	R4,R5,R6	ERJ-6ENF2003V	Panasonic	RES 200K OHM 1/8W 1% 0805 SMD
18	1	R7	ERJ-3EKF6041V	Panasonic	RES 6.04K OHM 1% 0603 SMD
19	1	R8	ERJ-6ENF2000V	Panasonic	RES 200 OHM 1/8W 1% 0805 SMD
20	1	R9	WSL2512R3000FEA	Vishay	RES 0.30 OHM 1W 1% 2512 SMD
21	1	R10	ERJ-6ENF9763V	Panasonic	RES 976K OHM 1/8W 1% 0805 SMD
22	1	R11	ERJ-3EKF1652V	Panasonic	RES 16.5K OHM 1/10W 1% 0603 SMD
23	1	R12	ERJ-3EKF9092V	Panasonic	RES 90.9K OHM 1/10W 1% 0603 SMD
24	2	R13,R15	ERJ-6ENF1004V	Panasonic	RES 1.00M OHM 1/8W 1% 0805 SMD

Table 8: 88EM8011 BOM (Continued)

Item	Qty	Ref	Manufacturer Part #	Manufacturer	Description
25	1	R14	ERJ-6ENF1002V	Panasonic	RES 10.0K OHM 1/8W 1% 0805 SMD
26	1	R-GATE	ERJ-3EKF10R0V	Panasonic	RES 10.0 OHM 1/10W 1% 0603 SMD
27	1	TP1	2508-2-00-44-00-00-07-0	Mil-Max	Swage Mount Terminal
28	1	T1	B82732F2601B001	EPCOS Inc.	EPCOS 07076
29	1	T2			BoostChoke with Secondary
30	1	U1	MRVL-88BL011	MARVELL	PFC CHIP

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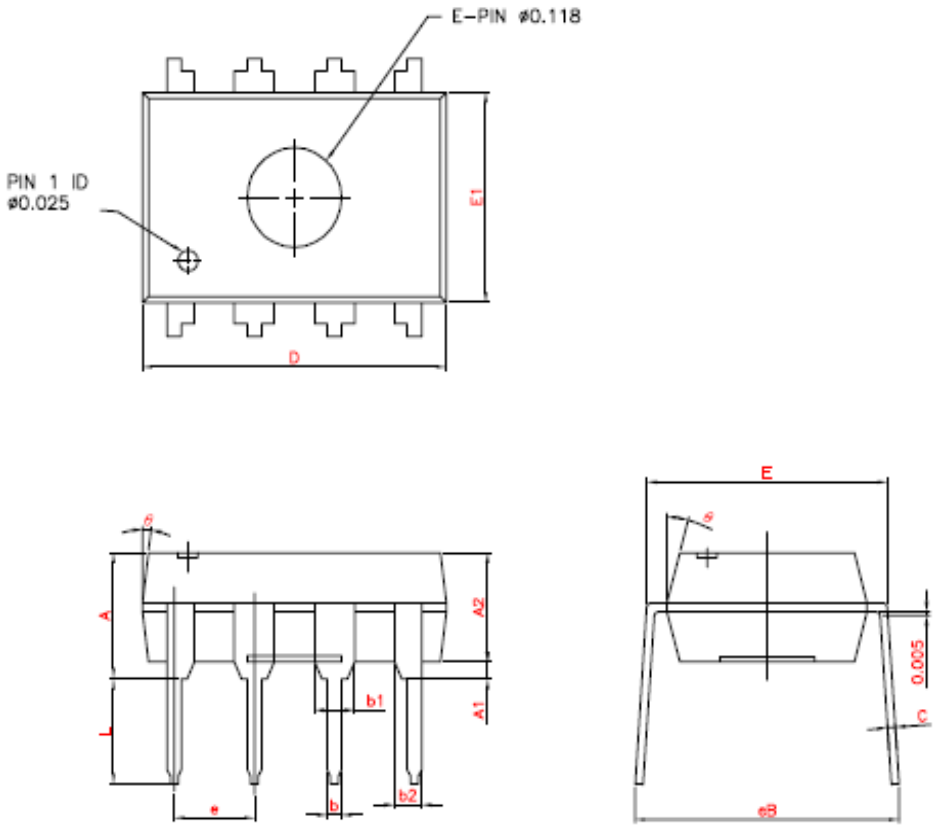
7 Mechanical Drawings

Figure 43: 8-Pin DIP Mechanical Drawing



Note

- Controlling dimension: inch
- Dimension shown do not include mold flash or other protrusion.
- The maximum allowable molding flash is 0.006” or protrusion on any side.
- See Section 8, Part Order Numbering/Package Marking, on page 55 for package marking and pin 1 location.

Table 9: 8-Pin DIP Dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.60	3.90	4.20	0.142	0.154	0.165
A1	0.38	--	--	0.015	--	--
A2	3.25	3.30	3.35	0.128	0.130	0.132
b	0.36	0.46	0.56	0.014	0.018	0.022
b1	1.45	1.60	1.73	0.057	0.063	0.068
b2	0.81	0.99	1.17	0.032	0.039	0.046
C	0.25	0.28	0.30	0.010	0.011	0.012
D	9.53	9.65	9.78	0.375	0.380	0.385
E	7.62	7.87	8.13	0.300	0.310	0.320
E1	6.22	6.35	6.48	0.245	0.250	0.255
e	--	2.54	--	--	0.100	--
L	3.18	0.71	3.43	0.125	0.028	0.135
eB	8.38	--	9.40	0.330	--	0.370
θ	8°	12°	14°	8°	12°	14°

Figure 44: 8-Pin SOIC Mechanical Drawing

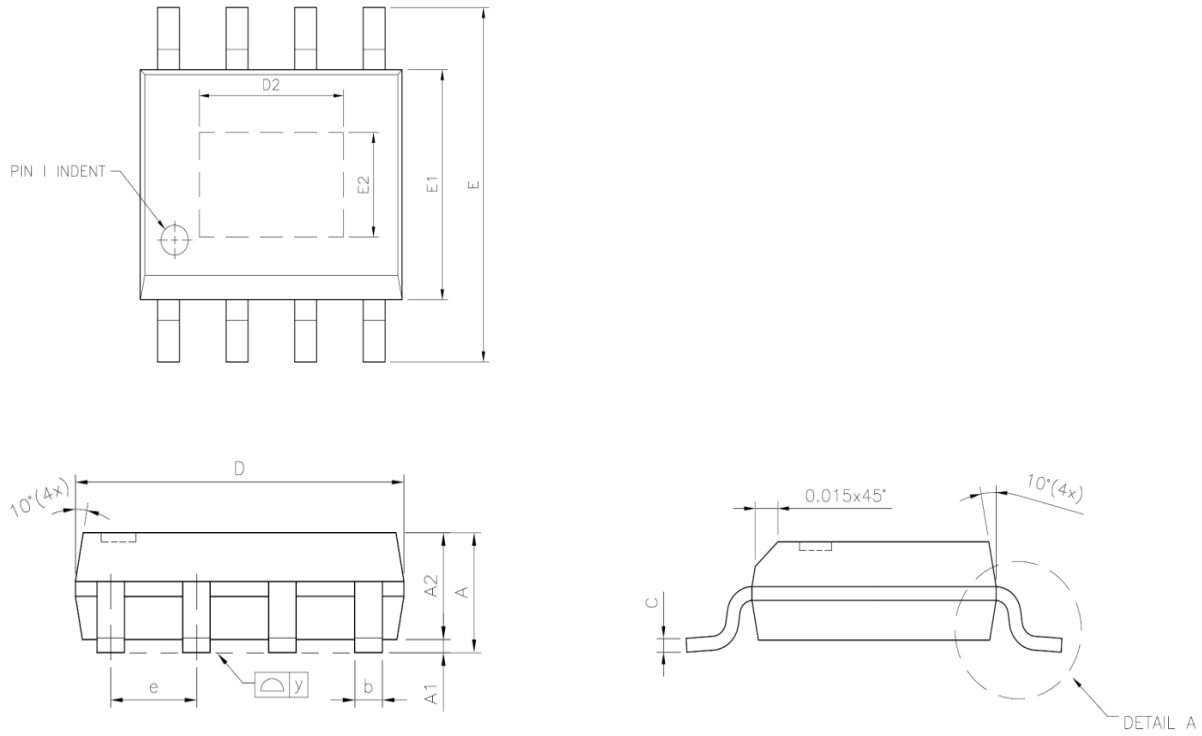


Table 10: Exposed PAD Dimensions (inch)

Exposed PAD Dimension (inch)						
PAD Size Option	D2			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
A.) 95x130mil	0.105	--	--	0.070	--	--

Table 11: 8-Pin SOIC Dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	--	0.25	0.004	--	0.010
A2	--	1.45	--	--	0.057	--
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	--	1.27	--	--	0.050	--
L	0.40	0.71	1.27	0.016	0.028	0.050
y	--	--	0.076	--	--	0.003
θ	0°	--	8°	0°	--	8°

Note

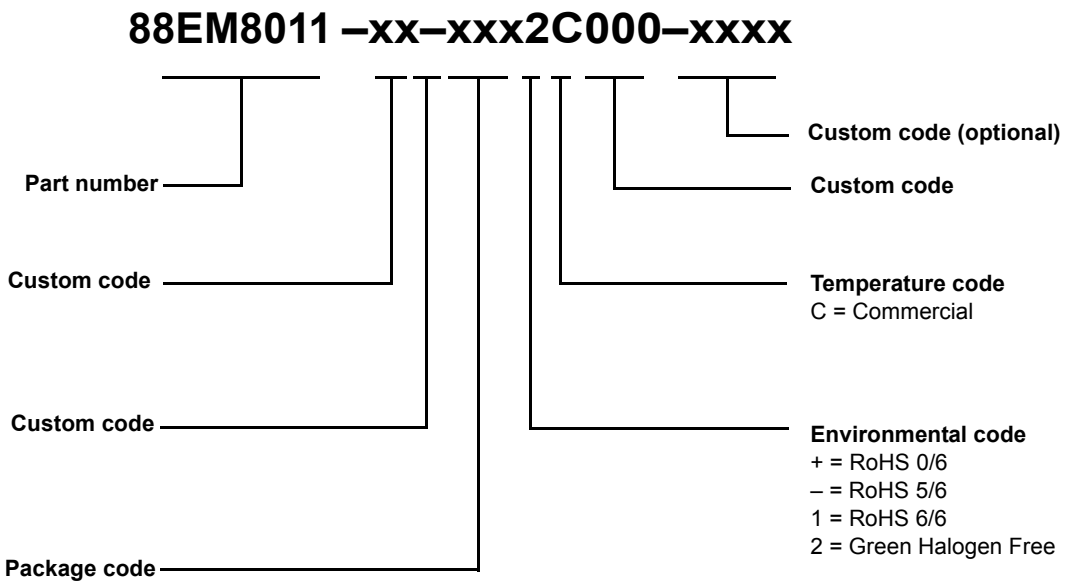
1. All dimensions in inch.
2. Lead frame material: Copper 194.
3. Dimension “D” does not include mold flash, tie bar burrs, and gate burrs. Dimension shall not exceed 0.006” (0.15 mm) per end. Dimension “E1” does not include interlead flash. Interlead flash shall not exceed 0.010” (0.25 mm) per side.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.003” (0.08 mm) total in excess of the “b” dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead to be 0.0028” (0.07 mm).
5. Tolerance: ±0.010” (0.25 mm) unless otherwise specified.
6. Otherwise dimension follow acceptable specification.

8 Part Order Numbering/Package Marking

8.1 Part Order Numbering

Figure 45 shows the part order numbering scheme for the 88EM8011 series. For complete ordering information, contact your Marvell FAE or sales representative.

Figure 45: 88EM8011 Sample Ordering Part Number



The standard ordering part number for the respective solution is shown in Table 12.

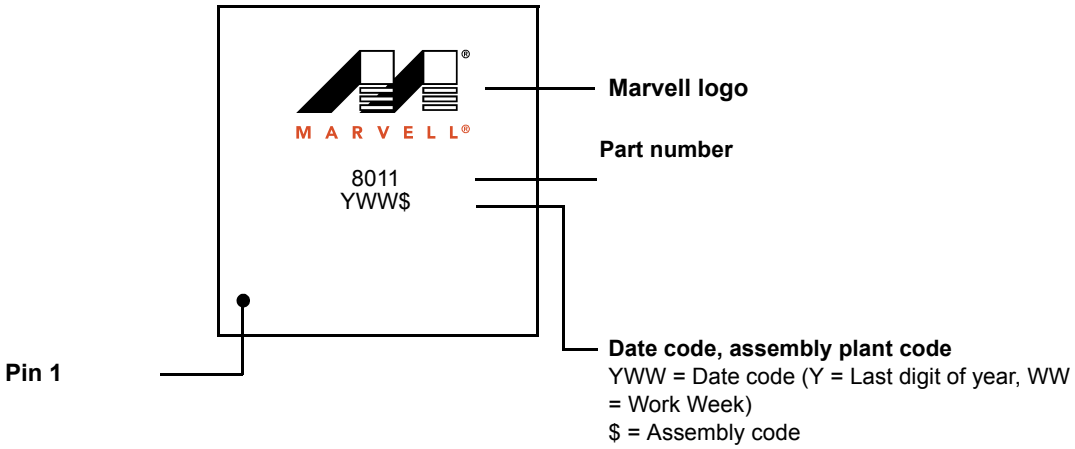
Table 12: 88EM8011 Part Order Options

Package Type	Part Order Number
8-Pin DIP Package	88EM8011-A0-PDA-C000-xxxx
8-Pin SOIC Package	88EM8011-A0-SAE2C000-xxxx

8.2 Package Markings

Figure 46 shows a typical package marking and pin 1 location for the part.

Figure 46: 88EM8011 Package Marking



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A Revision History

Table 13: Revision History

Document Type	Document Revision
Release	Rev. –
Draft	

Marvell Semiconductor, Inc.
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